Microprocessor System Data Transfer Interface Design: An Expert System Approach Using Signal Timing Behavioral Patterns

by

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A Dissertation Submitted in Partial Fulfillment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

in the Department of Electrical and Computer Engineering

We accept this dissertation as conforming
to the required standard

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Abstract

DAME (**D**esign **A**utomation of **M**icroprocessor-based systems using an **E**xpert system approach) is an expert system for configuring and designing a customized microprocessor systems from original specifications. This work deals with the development of the data transfer interface design module in DAME: the Interface Designer.

The automated Interface Designer is developed by extracting common features, functions and behavior of microprocessor components and representing them using knowledge representation techniques. The design is accomplished through pattern matching, by performing actions and procedures based on recognition of the standard behavior patterns of microprocessor component signals.

The development of the Interface Designer production system is divided into three parts: a hierarchial network of frames that represents the components, a hierarchial network of frames that represents the interface and a set of forward chaining rules that represents the design expertise. Equivalent abstraction levels are developed for the component model, interface model and design rules, allowing the design process to proceed using a top-down methodology.

The component behavior is abstracted at several levels. At the more abstract behavior level, the data transfer behavior is divided into a set of fundamental information transfers, namely the address, data, request, direction, type, delay, size and width information transfers. At the more detailed level, each information transfer is divided into state and timing information transfers, where state information represents the conceptual meaning of the state of a signal, and the timing information specifies when the state information is usable. Finally, the timing information is represented using a set of propagation delay invariant timing patterns. Only a limited number of timing patterns is required, thus allowing a limited number of design rules to accomplish the interface design.

Interface design is carried out by sub-dividing the interface into progressively more detailed interface sub-blocks, until eventually the interface is built up from a set of parameterized primitive circuits that represents the lowest level basic building blocks of an interface. The set of primitive circuits developed gives the Interface Designer the ability to connect signals based on the timing patterns. The timing behavior of the output of the interface is determined as a function of the primitive circuit parameters and the timing behavior of the input of the interface. Once the interface design is complete, the output

timing behavior of the interface is verified to assure that all component input timing constraints are satisfied.

Each of the primitive circuits developed is also given using VHDL. This allows the complete interface to be generated using VHDL code once the design is complete, permitting simulation for verification and synthesis for implementation of the interface. Several small test systems are designed and simulated to check the validity of the Interface Designer.

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Acknowledgments

I would like to thank Dr. Kin. F. Li for his help and guidance throughout the course of this work. I would also like to thank NSERC for providing financial support for this research.

Glossary

ALU	Arithmetic Logic Unit
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRL	Carnegie Representation Language
CRT	Cathode Ray Tube
DAME	Design Automation of Microprocessor-based systems using an Expert system approach
DIP	Dual In-line Package
DMA	Direct Memory Access
DSP	Digital Signal Processor
EPROM	Erasable Programmable ROM
HDL	Hardware Description Language
IO	Input / Output
IB	Interface Block
ISB	Interface Sub-Block
ISBP	Interface Sub-Block Primitive
LCC	Lead-less Chip Carrier
LSI	Large Scale Integration
MSI	Medium Scale Integration
NMOS	N-Type Metal Oxide Semiconductor
omp	Order of Magnitude Propagation delay
PAL	Programmable Array Logic
PGA	Pin Grid Array
P-M-S	Program-Memory-Switch
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
SSI	Small Scale Integration
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration